I claim:

1. A circuit for determining a time difference between edges of a first digital signal and of a second digital signal, the circuit comprising:

a first input for receiving a first signal;

a plurality of basic elements connected in succession and in series, each one of said plurality of basic elements having an input, a control input, and a storage unit with an output, said plurality of basic elements including a first basic element having an input connected to said first input for receiving the first signal, said input of each one of said plurality of basic elements, except that of said first basic element, connected to said output of a respective preceding one of said plurality of basic elements;

a second input for receiving a second signal, said second input connected to said control input of each one of said plurality of basic elements; each one of said plurality of basic elements, except for said first basic element, configured such that if the second signal has a first level, said storage unit will store a signal level that is already stored in said storage unit of an immediately preceding one of said plurality of basic elements, and if the second signal has

a second level, said storage element will retain a previously stored signal level; and

a plurality of comparator units having outputs, each one of said plurality of comparator units receiving the signal level stored by said storage elements of two adjacent ones of said plurality of basic elements, each one of said plurality of comparator units supplying a different event signal at said output thereof when two identical signal levels are received from said storage elements of two adjacent ones of said plurality of basic elements than when two different signal levels are received.

2. The circuit according to claim 1, wherein each one of said plurality of basic elements includes a first switching unit connected in series with said storage element, said first switching unit of each one of said plurality of basic elements having a control input defining said control input of a respective one of said plurality of basic elements.

3. The circuit according to claim 1, wherein each one of said plurality of comparator units is an exclusive or gate.

4. The circuit according to claim 1,comprising:

a delay unit having an input for receiving a reference signal and having an output;

said delay unit including a plurality of delay elements connected in series, each one of said plurality of delay elements having an output;

said delay unit including a plurality of second switching units, each one of said plurality of second switching units configured between the output of a respective one of said plurality of delay elements and said output of the delay unit; and

each one of said plurality of second switching elements having a control input connected to the output of a respective one of said plurality of comparator units.

5. The circuit according to claim 1, wherein said storage unit of each one of said plurality of basic units includes two inverters connected antiparallel.